

What is claimed is:

- 1 1. A four-transistor random access memory cell
2 comprising:
3 a first transistor of a first conductivity type having
4 a gate coupled to a word line and a source
5 coupled to a bit line;
6 a second transistor of the first conductivity type
7 having a gate coupled to a drain of the first
8 transistor and a source coupled to receive a
9 first voltage;
10 a third transistor of a second conductivity type having
11 a gate coupled to a drain of the second
12 transistor, a source coupled to receive a second
13 voltage and a drain coupled to the drain of the
14 first transistor; and
15 a fourth transistor of the second conductivity type
16 having a gate coupled to the drain of the first
17 transistor, a source coupled to receive the
18 second voltage and a drain coupled to the drain
19 of the second transistor.
- 1 2. The four-transistor random access memory cell as
2 in claim 1, wherein the first transistor further comprises a
3 bulk coupled to receive a third voltage.
- 1 3. The four-transistor random access memory cell as
2 in claim 2, wherein the first voltage is V_{dd} , the second
3 voltage is a ground voltage and the third voltage is V_{pp}
4 higher than V_{dd} .

1 4. The four-transistor random access memory cell as
2 in claim 2, wherein the first voltage is V_{dd} , the second
3 voltage is V_{bb} and the third voltage is V_{pp} higher than V_{dd} .

1 5. The four-transistor random access memory cell as
2 in claim 1, wherein the second transistor further comprises
3 a bulk coupled to receive a third voltage.

1 6. The four-transistor random access memory cell as
2 in claim 5, wherein the first voltage is V_{dd} , the second
3 voltage is a ground voltage and the third voltage is V_{pp}
4 higher than V_{dd} .

1 7. The four-transistor random access memory cell as
2 in claim 5, wherein the first voltage is V_{dd} , the second
3 voltage is V_{bb} and the third voltage is V_{pp} higher than V_{dd} .

1 8. The four-transistor random access memory cell as
2 in claim 1, wherein the first transistor further comprises a
3 bulk coupled to receive the first voltage.

1 9. The four-transistor random access memory cell as
2 in claim 8, wherein the first voltage is V_{dd} and the second
3 voltage is a ground voltage.

1 10. The four-transistor random access memory cell as
2 in claim 8, wherein the first voltage is V_{dd} and the second
3 voltage is V_{bb} .

1 11 The four-transistor random access memory cell as
2 in claim 1, wherein the second transistor further comprises
3 a bulk coupled to receive the first voltage.

1 12. The four-transistor random access memory cell as
2 in claim 11, wherein the first voltage is V_{dd} and the second
3 voltage is a ground voltage.

1 13. The four-transistor random access memory cell as
2 in claim 11, wherein the first voltage is V_{dd} and the second
3 voltage is V_{bb} .

1 14. The four-transistor random access memory cell as
2 in claim 1, wherein the first and second conductivity types
3 are respectively P and N type.

1 15. A random access memory cell comprising:
2 a first transistor of a first conductivity type having
3 a gate coupled to a word line and a source
4 coupled to a bit line;
5 a second transistor of a second conductivity type
6 having a source coupled to receive a second
7 voltage and a drain coupled to the drain of the
8 first transistor;
9 a diode having an anode coupled to the drain of the
10 first transistor and a cathode coupled to receive
11 a first voltage; and
12 an inverter having an input terminal coupled to the
13 drain of the first transistor and an output
14 terminal coupled to a gate of the second
15 transistor.

1 16. The random access memory cell as in claim 15,
2 wherein the inverter comprises:

3 a third transistor of the first conductivity type
4 having a gate coupled to the drain of the first
5 transistor and a source coupled to receive the
6 first voltage; and
7 a fourth transistor of the second conductivity type
8 having a gate coupled to the drain of the first
9 transistor, a source coupled to receive the
10 second voltage and a drain coupled to the drain
11 of the third transistor.

1 17. The random access memory cell as in claim 16,
2 wherein the first and third transistor each comprise a bulk
3 coupled to receive a third voltage.

1 18. The random access memory cell as in claim 17,
2 wherein the first voltage is V_{dd} , the second voltage is a
3 ground voltage and the third voltage is V_{pp} higher than V_{dd} .

1 19. The random access memory cell as in claim 17,
2 wherein the first voltage is V_{dd} , the second voltage is V_{bb}
3 and the third voltage is V_{pp} higher than V_{dd} .

1 20. The random access memory cell as in claim 16,
2 wherein each of the first and third transistors comprises a
3 bulk coupled to receive the first voltage.

1 21. The random access memory cell as in claim 20,
2 wherein the first voltage is V_{dd} and the second voltage is a
3 ground voltage.

1 22. The random access memory cell as in claim 20,
2 wherein the first voltage is V_{dd} and the second voltage is
3 V_{bb} .

1 23. The random access memory cell as in claim 16,
2 wherein the diode is formed by a junction between the bulk
3 and drain of the first transistor.

1 24. A memory device comprising:
2 a plurality of memory cells wherein data is read from
3 and written into each of the memory cells through
4 bit lines by control signals on word lines, each
5 of the memory cells comprising:
6 a first transistor of a first conductivity type
7 having a gate coupled to one of the word
8 lines and a source coupled to one of the bit
9 lines;
10 a second transistor of the first conductivity type
11 having a gate coupled to a drain of the
12 first transistor and a source coupled to
13 receive a first voltage;
14 a third transistor of a second conductivity type
15 having a gate coupled to a drain of the
16 second transistor, a source coupled to
17 receive a second voltage and a drain coupled
18 to the drain of the first transistor; and
19 a fourth transistor of the second conductivity
20 type having a gate coupled to the drain of
21 the first transistor, a source coupled to
22 receive the second voltage and a drain

23 coupled to the drain of the second
24 transistor.

1 25. The memory device as in claim 24, wherein the
2 first transistor further comprises a bulk coupled to receive
3 a third voltage.

1 26. The memory device as in claim 25, wherein the
2 first voltage is V_{dd} , the second voltage is a ground voltage
3 and the third voltage is V_{pp} higher than V_{dd} .

1 27. The memory device as in claim 25, wherein the
2 first voltage is V_{dd} , the second voltage is V_{bb} and the third
3 voltage is V_{pp} higher than V_{dd} .

1 28. The memory device as in claim 24, wherein the
2 second transistor further comprises a bulk coupled to
3 receive the third voltage.

1 29. The memory device as in claim 28, wherein the
2 first voltage is V_{dd} , the second voltage is a ground voltage
3 and the third voltage is V_{pp} higher than V_{dd} .

1 30. The memory device as in claim 28, wherein the
2 first voltage is V_{dd} , the second voltage is V_{bb} and the third
3 voltage is V_{pp} higher than V_{dd} .

1 31. The memory device as in claim 24, wherein the
2 first transistor further comprises a bulk coupled to receive
3 the first voltage.

1 32. The memory device as in claim 31, wherein the
2 first voltage is V_{dd} , the second voltage is a ground voltage
3 and the third voltage is V_{pp} higher than V_{dd} .

1 33. The memory device as in claim 31, wherein the
2 first voltage is V_{dd} , the second voltage is V_{bb} and the third
3 voltage is V_{pp} higher than V_{dd} .

1 34. The memory device as in claim 24, wherein and the
2 second transistor further comprises a bulk coupled to
3 receive the first voltage.

1 35. The memory device as in claim 34, wherein the
2 first voltage is V_{dd} , the second voltage is a ground voltage
3 and the third voltage is V_{pp} higher than V_{dd} .

1 36. The memory device as in claim 34, wherein the
2 first voltage is V_{dd} , the second voltage is V_{bb} and the third
3 voltage is V_{pp} higher than V_{dd} .

1 37. The memory device as in claim 24, wherein the
2 first and second conductivity types are P and N type
3 respectively.

1 38. A memory device comprising:
2 a plurality of memory cells wherein data is read from
3 and written into each of the memory cells through
4 bit lines by control signals on word lines, each
5 of the memory cells comprising:
6 a first transistor of a first conductivity type having
7 a gate coupled to a word line and a source
8 coupled to a bit line;

9 a second transistor of a second conductivity type
10 having a source coupled to receive a second
11 voltage and a drain coupled to the drain of the
12 first transistor;
13 a diode having an anode coupled to the drain of the
14 first transistor and a cathode coupled to receive
15 a first voltage; and
16 an inverter having an input terminal coupled to the
17 drain of the first transistor and an output
18 terminal coupled to a gate of the second
19 transistor.

1 39. The memory device as in claim 38, wherein the
2 inverter further comprises:
3 a third transistor of the first conductivity type
4 having a gate coupled to the drain of the first
5 transistor and a source coupled to receive the
6 first voltage; and
7 a fourth transistor of the second conductivity type
8 having a gate coupled to the drain of the first
9 transistor, a source coupled to receive the
10 second voltage and a drain coupled to the drain
11 of the third transistor.

1 40. The memory device as in claim 39, wherein the
2 first and third transistors each comprise a bulk coupled to
3 receive a third voltage.

1 41. The memory device as in claim 40, wherein the
2 first voltage is Vdd, the second voltage is a ground voltage
3 and the third voltage is VPP higher than Vdd.

1 42. The memory device as in claim 40, wherein the
2 first voltage is Vdd, the second voltage is V_{bb} and the
3 third voltage is VPP higher than Vdd.

1 43. The memory device as in claim 39, wherein the
2 first and third transistors each comprise a bulk coupled to
3 receive the first voltage.

1 44. The memory device as in claim 43, wherein the
2 first voltage is Vdd and the second voltage is a ground
3 voltage.

1 45. The memory device as in claim 39, wherein the
2 diode is formed by a junction between the bulk and drain of
3 the first transistor.

1 46. A 4T-SRAM cell in a SRAM array having pairs of a
2 first and second bit line, and a first and second word line,
3 comprising:
4 a first transistor of a first conductivity type having
5 a gate coupled to one of the first word lines and
6 a source coupled to one of the first bit lines;
7 a second transistor of the first conductivity type
8 having a gate coupled to a drain of the first
9 transistor and a source coupled to receive a
10 first voltage;
11 a third transistor of a second conductivity type having
12 a gate coupled to a drain of the second
13 transistor, a source coupled to receive a second
14 voltage and a drain coupled to the drain of the
15 first transistor; and

16 a fourth transistor of the second conductivity type
17 having a gate coupled to one of the second word
18 lines, a source coupled to one of the second bit
19 lines and a drain coupled to the gate of the
20 third transistor.

1 47. The 4T-SRAM cell as in claim 46, wherein bulks of
2 the first and fourth transistor are respectively coupled to
3 receive the first and second voltage.

1 48. The 4T-SRAM cell as in claim 46, wherein the first
2 and second conductivity types are respectively P and N type.